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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/341,633	07/15/1999	SATOSHI NAKAMURA	1152-237P	5369

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BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

EXAMINER	
SINGH, DALIP K	

ART UNIT	PAPER NUMBER
2676	19

DATE MAILED: 12/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/341,633	NAKAMURA ET AL.	
	Examiner	Art Unit	
	Dalip K Singh	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to Interview conducted on April 28, 2004 with Catherine M. Voisnet, attorney of record, Examiner Singh and Supervisory Examiner Matthew Bella. As a result of the interview, the finality of the last office action has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of U.S. Patent No. 5,771,031 to Kinoshita et al.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3 and 6 are rejected under 3 5 U. S.C. 103(a) as being unpatentable over U.S. Patent No. 5,909,205 to Furuhashi et al. in view of U.S. Patent No. 5,771,031 to Kinoshita et al.

a. Regarding claim 1, Furuhashi et al. **teaches** a frame and line memory control circuit 112 that controls the readout of the necessary display data from the line memory to display it on the screen as part of the liquid crystal display control device (Figure 1, col. 6, lines 54-67; col. 7, lines 30-34). Furuhashi et al. **teaches** a main memory (frame memory 110), a data processing circuit (A/D convertor 104). See figure 1, col. 7, lines 30-34; Furuhashi et al. does teach a frame/line memory control circuit (frame memory write control circuit 214, frame memory read control circuit 215, line memory write control circuit 216 and lime memory read control circuit 217, See Fig. 2, col. 9, lines 59-67) that controls the transfer and storage of the display data from main memory (frame memory 110) to line memory (line memory 111) and the readout of the necessary display data from line memory to display it on the screen; and the storage of display data in

main memory (frame memory 110). Furuhashi et al. **fails to disclose** a number of line memories being read out by way of specifying the address of the display data for one line, and specifically, selection of a line memory from a number of line memories. Kinoshita et al. **discloses** a liquid crystal controller with a data distribution circuit with a selector WS, memories M1 to M3, and a selector RS, the selector WS selects one of the memories M1, M2 and M3. Each of the memories M1 to M3 has one hundred memory areas of 18 bits thus plurality of line memories are being accessed as they are being selected by the selector (Fig. 4, lines 1-67). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify Furuhashi with the "plural memories with a selector" as taught by Kinoshita et al. **because** it is possible to increase the data items and the word length without increasing the storage capacity of the memories resulting in cost reduction (col. 16, lines 25-49).

b. Regarding claim 2, Furuhashi teaches display data (line memory read data 116) being read out from the said line memory (line memory 111) and displayed on the screen. See col. 7, lines 66-67 and col. 8, lines 1-3.

c. Regarding claim 3, Furuhashi does not explicitly teach a data buffer memory for storing the display data to be utilized repeatedly. However, it would have been obvious to one of ordinary skill in the art at the time invention was made to provide a data buffer memory in front of line memory of Furuhashi because such data buffering is well known in the data processing art for such purposes as retiming the data.

d. Regarding claim 6, Furuhashi discloses an A/D Convertor 104. Furuhashi does not disclose a plurality of conversion processing circuit. However, it would have been obvious to one of ordinary skill in the art at the time invention was made to provide a plurality of conversion processing circuit to include various data formats as in the instant claim because this would make the device more flexible and useful.

4. Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,909,205 to Furuhashi et al. in view of U.S. Patent No. 5,771,031 to Kinoshita et al as applied to claim 1 and further in view of U. S. Patent No. 5,808,629 to Nally et al.

a. Regarding claim 4, Nally teaches a first buffer memory for storing the display data read out from said main memory, a second buffer memory for storing the display data read out from said first buffer memory. See col. 14, line 13-15. Nally does not disclose an address counter for counting the readout address and the write address of said first and the second buffer memories. However, Nally teaches an input and output address counter as separate entities. See figure 7, col. 14, lines 50-51; col. 15, lines 2021. It would have been obvious to one of ordinary skill in the art at the time invention was made to combine the input and output address counter into a single block to reduce logic. Furuhashi teaches an enlargement processing control circuit 120 which can perform the processing of expansion, contraction and skip and storing of the data in said line memory. See figure 1, col. 7, lines 66-67; col. 8, lines 1-3. It would have been obvious to one of ordinary skill in the art at the time invention was made to modify Furuhashi-Kinoshita combination line memories by including a first and a second buffer of Nally because this would reduce the jumping or splitting of fast moving objects or images on the display screen.

b. Regarding claim 5, Nally teaches an input and output address counter which are run in a predetermined order. See figure 7, col. 14, lines 2-5. Furuhashi does not teach an input and output address counter, which run in a predetermined order. It would have been obvious to one of ordinary skill in the art at the time invention was made to include the input and output address counters of Nally in Furuhashi-Kinoshita combination because this would ensure a synchronous data transfer between line memory and display panel.

4. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,909,205 to Furuhashi et al. in view of U.S. Patent No. 5,771,031 to Kinoshita et al. as applied to claim 1 above and further in view of U.S. Patent No. 6,252,563 to Tada et al..

a. Regarding claim 7, Tada teaches a program memory and a data memory connected to a CPU. See figure 1, col. 4, lines 21-22. Furuhashi-Kinoshita combination does not teach a separate program and data memory. However, it would have been obvious to one of ordinary skill in the art at the time invention was made to include the Tada's program and data memory in Furuhashi-Kinoshita combination because this would reduce the accesses to the main memory and reduce latency towards the display panel.

b. Regarding claim 8, Tada teaches a program memory and data memory. See figure 1, col. 4, lines 21-22. Tada does not teach a main memory providing data to these two memory locations. However, it would have been obvious to one of ordinary skill in the art at the time invention was made to provide for a data flow between the display controller and the program and data memory because this would enable a means to update the application code for different revisions of software/firmware which is a very well known procedure in the software applications.

5. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,909,205 to Furuhashi et al. in view of U.S. Patent No. 5,771,031 to Kinoshita et al. as applied to claim 1 above and further in view of Selwan et al. U.S. Patent No. 5,526,025.

a. Regarding claim 9, Selwan teaches a method of run length tagging for repetitive memory. See col. 6, lines 48-67; col. 7, lines 1-28. Selwan does not teach adding the line information, which shows which line the data is to be used when storing the display data in the said line memory. However, it would have been obvious to one of ordinary skill in the art at the time invention was made to add the line information showing in which line

the data is to be used when storing the display data in said line memory, which is a process taught by Selwan, and modify Furuhashi-Kinoshita combination line memory data accordingly because this would serve as a comparator and thus reduce the possibility of fetching the wrong data from a particular line memory and this technique of tagging a data word for subsequent comparison or error-checking is well known in the data processing art.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Dalip K. Singh** whose telephone number is **(703) 305-3895**. The examiner can normally be reached on Mon-Thu (8:00AM-6: 30PM) Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Matthew Bella**, can be reached at **(703) 308-6829**.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

dks

November 24, 2004

MATTHEW C. BELLA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600